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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,165	SAKIYAMA ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-14* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for continued examination filed 07 June 2007 and the claims filed 21 May 2007 have been received and entered in the case. Claims 6-16 are considered below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Shoji (USPN 4,670,670).

With respect to claim 6, Shoji discloses "a semiconductor integrated circuit (circuit of Fig. 1), comprising:

a main circuit (circuit with body biased by the signal at 40, not shown in Fig. 1) including a plurality of MOS transistors of a MOS structure in which a source potential and a substrate potential are separated from each other (the circuit is composed of MOS transistors), and operating while receiving a predetermined operating power supply voltage (VDD); and

a substrate potential control circuit (12, 13 and 20-29) for controlling the substrate potential (P-TUBs) of a MOS transistor in the main circuit (the signal at 41 biases the substrate, i.e., P-TUB, of the main circuit) so that an actual saturation current

value of the MOS transistor is equal to a target saturation current value that is sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit, the substrate potential control circuit (the circuit of Fig. 1 is connected exactly as recited and as shown in Fig. 5 of the instant application and therefore the circuit operates as recited), including:

a constant current generation circuit (22);

a current-voltage conversion circuit including a MOS transistor provided therein (50) and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein, which for converting a constant current value of the constant current generation circuit to a voltage value (the output 50, i.e., the pad of 13, is combined with the output of 22 to convert the current output from 22 to a voltage that which changes according to the substrate potential of 50); and

a differential amplifier circuit (20) for controlling a substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit (20 receives the combined output of 22 and 50 as well as the operating power supply VDD via 23 and 24. Furthermore 20 controls the substrate voltage of 50, therefore 20 controls the substrate to be equal to VDD due to the feedback of the output of 50 and the supply voltage being input to 20), wherein the substrate potential control circuit controls the substrate potential of each of the MOS transistors in the main circuit so that the substrate potential is equal to the substrate

potential of the current-voltage conversion circuit controlled by the differential amplifier circuit (similar to that of 50, the substrate of the main circuit is controlled by the output of 20. Thus, the main circuit has a substrate potential that is equal to the substrate voltage of the main circuit is equal to the substrate voltage of 50).

With respect to claim 7, Shoji discloses, VDD is any desired operating voltage which may vary in any desired range, since 22 is connected to VDD its current value will change in proportion to a change in VDD.

With respect to claim 8, Shoji discloses a linear change in the current output by 22 with respect to the change in VDD, since the output of 22 will directly flow the increase in VDD.

With respect to claim 9, Shoji discloses, that VDD is any desired operating voltage. Thus, VDD many be any of a polarity of operating voltage (i.e., 3 Volts, 5 Volts, etc.). Furthermore, since 22 is connected to VDD its current value will change in proportion to a change in VDD, wherein the change of current output from 22 will be linear with respect to the supply voltage change.

Claims 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaenel et al. (USPN 5,682,118).

With respect to claim 13, Kaenel et al. discloses in Fig. 7 a semiconductor integrated circuit, comprising:

a main circuit including a plurality of MOS transistors of a MOS structure (119), and operating while receiving an operating power supply voltage (119 operates when it receives the power supply of Vlog); and

a power supply voltage control circuit for controlling the operating power supply voltage supplied to the main circuit (control circuits 104, 101 and 102 operate to output Vlog), wherein:

a target saturation current value of the MOS transistors that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage is set in the power supply voltage control circuit (Vlog is output to 119 by the control circuits of 104, when control circuits 101,and 102 indicate that the target saturation currents output by 111 and 118 are met. VBp, and VBn are then adjusted, according to Vlog/2 and the current output by 111 and 118. VBp and VBn are output to 104 to control Vlog to be output to 119. Vlog, VBn, and VBp control the operating speed of the transistors of 119, see Col. 8 lines 63-67, Col. 9 lines1-3); and

the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current value (note that104 supplies the desired voltage Vlog to 119, which is controlled by 104, 101 and 102. Thus the circuits of 119 receive a regulated voltage Vlog, and regulated back bias voltages Vbn and Vbp to maintain the target threshold, i.e., saturation current of the circuits of 119)."

With respect to claim 14, Kaenel et al. discloses, "the semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is a target saturation current value of an NMOS transistor or that of a PMOS transistor from among the MOS transistors of the main circuit, or is an average value between the target saturation current values of the NMOS and PMOS transistors."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (USPAPN 2004/0070440) in view of Forbes et al. (USPN 6,456,157).

With respect to claim 6, Tang et al. discloses in Figs. 1-6, "a semiconductor integrated circuit (circuit of Fig. 1, Fig. 3 or Fig. 4), comprising:

a main circuit including a plurality of MOS transistors of a MOS structure (108 is a main circuit that contains multiple MOS transistors) in which a source potential (Local Vcc) and a substrate potential (Vout') are separated from each other, and operating while receiving a predetermined operating power supply voltage; and

a substrate potential control circuit (100, and circuit that outputs Vbs) for controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation

current value that is sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit (the saturation current of the MOS transistors of 108 will be equal to the desired saturation currents of Vbs),

the substrate potential control circuit, including:

a differential amplifier (102) circuit for controlling a substrate potential (Vout') of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit (Vout' is fed back to the inverting terminal of 102, so as to control the output of Vout' in accordance with Vbs, i.e., output of substrate control circuit)

wherein the substrate potential control circuit controls the substrate potential of each of the MOS transistors in the main circuit so that the substrate potential is equal to the substrate potential of the current-voltage conversion circuit controlled by the differential amplifier circuit (102 controls Vout' so that Vout' is applied to the body of each MOS transistor, so that each MOS transistor of 108 has a body bias voltage of each MOS transistor is equal to Vbs)."

Tang et al. further discloses a generic substrate signal Vbs that represents "a difference between a body and a source voltage (see lines 1-3 of paragraph [0010])"

What Tang et al. fails to teach is "the substrate potential control circuit, including:

a Constant Current generation Circuit;

a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value;"

However, Forbes et al discloses in Fig. 3 and Fig. 8, a substrate potential control circuit, including (Fig. 3, or Fig. 8):

a Constant Current generation Circuit (110);

a current-voltage conversion circuit (101) including a MOS transistor (101) provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein (the current to voltage conversion circuit of 100 characteristics of 101 change according to the substrate potential applied at 108) for converting a constant current value of the constant current generation circuit to a voltage value (101 converts current from 110 to the back bias voltage of VBG)". Fig. 8 of Forbes et al. discloses an n-well biasing circuit similar to that of the p-well biasing circuit of Fig. 3. Note further that Fig. 3 and Fig. 4 output a bias voltage that is a difference between a body (body of 101 of Fig. 3, or body of 202 of Fig. 8) and a source (Vdd with constant current source 110 of Fig. 3, and ground with the constant current source of Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the generic body bias voltage generating circuits that output Vbs in Figs. 1, 3 and 4 of Tang et al. with the specific body bias generation circuits of Fig. 3 and Fig. 8 of Forbes et al. for the purpose of having a simply constructed body bias

generating circuit that outputs a body bias voltage that is the "difference between a source and a body", and have increased flexibility in setting threshold voltages (see lines 8-9 of the Abstract of Forbes et al.).

With respect to claim 7, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is proportional to the operating power supply voltage value within the operating voltage range (the target saturation current changes in proportion to supply voltage changes, This is because Vout' is controlled by both Vcc and Vbs input to 102. Additionally, see Fig. 5 and lines 5-11 of paragraph [0017] clearly as Vcc is increased Vout', i.e., LBG output, is increased in proportion)."

With respect to claim 8, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range (it can be seen in Fig. 5 that as Vcc is increased Vout', i.e., LBG output, is also increased linearly (i.e., as Vcc is increased by .1 Volts Vout', i.e., LBG output, also increases by .1 Volts)."

With respect to claim 9, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges (it can be seen that multiple Vcc supply voltages are used in Fig. 5);

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit (it can be see in Fig. 5 that the relationship between Vout', i.e., LBG Output, and Vcc is linear, as Vcc increases Vout' also increases in proportion); and

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range (it can be seen in Fig. 5 that the relationship between each voltage supply, Vout' and Vbs is different, i.e., in each relationship Vout' is larger at each Vbs voltage for each supply voltage Vcc)."

With respect to claim 11, the above combination discloses the semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the actual saturation current value of the MOS transistors of the main circuit (it can be seen that the output of the Vbs signal is actually smaller than that of the required saturation of the MOS circuits of 108). Thus, Tang et al. requires differential amplifier 102, and output buffer 104, to increase the gain of the Vbs signal to be provided as the Vout' signal, and the variation in current of the Vbs generation circuit is less than the actual required saturation current of 108 controlled by Vout', see lines 1-7 of paragraph [0017].

Claims 10 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (USPAPN 2004/0070440) and Forbes et al. (USPN 6,456,157) as applied to claims 6-9 above, and further in view of Bowden (USPN 4,427,935).

The combination of Tang et al. and Forbes et al. fails to disclose the constant current generation circuit generates a plurality of constant current values, and selectively outputs one of the plurality of constant current values.

However, Bowden discloses in Fig. 1, a constant current source that corrects variations in a supply source, thus providing a stable constant current output, and is selectable to output a desired current source"

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the generic current source 110 of Fig. 3 of Forbes et al. (and the generic current source of Fig. 8) with the specific constant current source of Fig. 1 of Bowden for the purpose of having a constant current source that compensates for variations in the supply voltage. Thus, the above combination discloses, all of the recited limitations of claim 6, since selector 14 outputs a plurality of voltages to be generated as one of multiple constant currents outputs.

With respect to claim 12, the above combination discloses, all of the recited limitations of claim 12, since Bowden's constant current is adjustable (according to the variable resistor connected to 21 and selector 14) to select a desired current that is constant and stable through its compensation circuits.

Response to Arguments

The argument that the combination of Tang et al. (USPAPN 2004/0070440) and Forbes (USPN 6,456,157) fails to disclose a current-voltage conversion circuit including a MOS transistor and having "current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor" and having "a differential amplifier circuit" as recited in claim 6 is not persuasive. First, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Claims 6-9 and 11 are rejected under the combination of both Tang et al. and Forbes, not each reference alone. For instance, Fig. 3 of Forbes discloses an NMOS bias voltage producing circuit, which includes a current to voltage conversion circuit (110 with 101) of a MOS transistor (101) a constant current source (110) wherein the current-voltage conversion characteristics change according to the substrate potential of the MOS transistor (clearly the output of Fig. 3, i.e., current-voltage characteristics, of Fig. 3 change according to the substrate potential, i.e., VBG of Fig. 3, see Figs. 5 and 7). With respect to the motivation for combining Forbes and Tang, Tang discloses that the bias voltage Vbs is generated by a difference between a body and a source voltage. Furthermore, it can be seen that the bias voltages of Figs. 3 and 8 of Forbes are generated by a difference between a body and source voltage. Therefore, it would have been obvious to replace the generic bias generator of Tang with the specific bias generator of Forbes.

With respect to the differential amplifier as recited in claim 6, it can be seen in Fig. 3 and Fig. 4 that Tang et al. discloses such a differential amplifier (i.e., 100 of Fig. 3 of Tang et al.), which controls the substrate potential (i.e., output of 200, Vbs of Fig. 3 of Tang et al., i.e., output of Fig. 3 of Forbes as modified) to be equal to the predetermined operating power supply (Local Vcc) of the main circuit (300), due to the regulation/buffering of Vbs (i.e., output of Fig. 3 of Forbes et al. as modified) by circuit 100 of Fig. 3 of Tang et al, Vbs will be controlled to be equal to Local Vcc at the output of 100.

The argument that Kaenel (USPN 5,682,118) fails to disclose the power supply voltage control circuit controlling a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors in the main circuit is equal to the target saturation current is not persuasive. It can be seen in Fig. 7 of Kaenel that Vlog (i.e., operating power supply voltage of the main circuit 119) is maintained by the control circuit (i.e., circuits that output VBn and. VBp), due to the control circuit's control of Vlog generating circuit 104 (i.e., VBn and VBp control slave circuit 104 that outputs Vlog responsive to VBn and VBp). Furthermore, the control circuit controls the substrate potential of the circuit 119 (i.e., VBn and VBp are input to 119), and because Kaenel's circuit operates to control the threshold of the transistors of 119, one of ordinary skill in the art would understand that such control of a transistor's threshold correlates to the control of the transistor's saturation current. Therefore, due to the regulated control of Vlog and the regulated substrate potential of the transistors of circuit 119 provided by the control circuit of Fig.

7, Kaenel's circuit operates as recited in claim 13. Furthermore, it can be seen that Kaenel's substrate control circuit has essentially the same structure/functionality as Applicant's present invention as claimed, and thus Kaenel's circuit will operate as recited in claim 13.

Allowable Subject Matter

Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 15, clearly it can be seen that Kaenel et al. does not disclose "the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage supplied to the main circuit". In fact, Fig. 10 discloses a logarithmic relationship between the current and supply voltage.. Thus Kaenel et al. teaches away from a linear relationship between the saturation current and the supply voltage. Furthermore, there is no disclosure or motivation provided to have a linear relationship between the supply voltage and saturation current. It can be seen that Tang et al. discloses in Fig. 5 a linearly relationship between supply voltage bias voltage, and Vout'. Thus, the saturation current and supply voltage would have an inherent linear relationship. However, Tang fails to disclose the specific "power supply voltage control circuit" of as recited in claim 13. Thus, Tang fails to disclose all the recited limitations of claim 15. Therefore, claim 15 is allowable.

With respect to claim 16, it can be seen that claim 16 recites the same linear relationship between the target saturation current value and the operating power supply voltage value of claim 15. Thus, claim 16 is allowable for at least the same reasons as claim 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
August 15, 2007

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816